ANNUAL REPORT

Novel SiC High Power IC Tehnology

Supported Under Grant # N00014-98-1-0534
Office of Naval Research
Funded by DARPA/ETO
Program Scientific Officer: Dr. Dan Radack
Program Monitor: Dr. George J. Campisi
Report for the Period of
January 1, 1999 through December 31, 1999

Principal Investigator: Professor B. Jayant Baliga

Department of Electrical and Computer Engineering
Power Semiconductor Research Center
North Carolina State University
Campus Box 7924
Raleigh, North Carolina 27695-7924

19991229 045

REPORT DOCUMENTATION PAGE

1. AGENCY USE ONLY (Leave Blank)	2. REPORT DATE 1112/31/99	3. REPORT TYPE AND DATES COVERED Annual (January 1, 1999 - December 31, 1999)

4. TITLE AND SUBTITLE
Novel SiC High Power IC Technology
4H SiC Lateral RESURF Devices

5. FUNDING NUMBERS
PR Number 98PRO5288-00

6. AUTHORS
Pronita Mehrotra, Aravind Venkateswaran, B. J. Baliga

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
North Carolina State University
Hillsborough Sstreet
Raleigh, NC 27695

8. PERFORMING ORGANIZATION REPORT NUMBER
N00014-98-1-0534

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Sponsoring: ONR, Code 254: 800 North Quincy Street, Arlington, VA 22217-5660
Monitoring: Administrative Grants Officer, ONR Regional Office Atlanta
Regional Office, Suite 4R15, 100 Alabama Street NW
Atlanta, GA 30303-3104

10. SPONSORING / MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION / AVAILABILITY STATEMENT
Approved for Public Release; Distribution Unlimited

12b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)

The goal of this project is to develop a silicon carbide technology which is similar to that used today for manufacturing silicon power ICs. Silicon high voltage devices are integrated together with CMOS circuits by using the RESURF concept to create lateral structures with high voltage handling capability. In the case of silicon, the RESURF region must have an optimum charge of about 1×10^{12} cm^{-2}. Due to the higher breakdown electric field strength of SiC, it can be expected that the optimum dose for SiC devices will also be larger leading to lower on resistances. Our analysis performed using two-dimensional numerical simulations has demonstrated that the optimum RESURF dose for SiC is an order of magnitude greater than that for silicon. We have also found that it is better to use silicon nitride instead of silicon dioxide as the field dielectric to avoid high electric fields. In order to confirm our analysis, we have defined a 11 mask planar process for SiC based upon ion implantation to form all the device structural regions. We have completed the design of a mask set with 47 structures consisting of high voltage rectifiers and power MOSFETs with both inversion channels and accumulation channels together with CMOS transistors. The fabrication of devices has been starting using 4 wafers procured from CREE Research Inc. with 10 micron thick P-type layers grown on P+ substrates.

14. SUBJECT TERMS
RESURF, Silicon Carbide, MOSFET, nitride, on-resistance, excessive field crowding,

15. NUMBER OF PAGES
15

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT Unclassified	18. SECURITY CLASSIFICATION OF THIS PAGE Unclassified	19. SECURITY CLASSIFICATION OF ABSTRACT Unclassified	20. LIMITATION OF ABSTRACT SAR

TABLE OF CONTENTS

4H SiC Lateral RESURF Devices

I.   Introduction

High Power ICs for applications in combat vehicles, more electric aircraft, naval ships and commercial vehicles require the development of high voltage devices in SiC and an appropriate isolation technique. To support high voltages in lateral SiC power devices, a uniform electric field is required in the drift region as governed by the RESURF (Reduced SURface Field) principle. RESURF eliminates surface breakdown in lateral devices by preventing electric field at the surface from reaching the critical value and hence higher breakdown voltages can be obtained. For isolation, sub-surface ion-implantation of a neutral impurity like Argon has been proposed by us. The deep levels caused by ion-implantation damage create high resistivity layers in SiC even for moderate doses of 1×10^{15} /cm^2 . Therefore this technique would be more cost effective as compared to Si SIMOX technology which requires oxygen doses of 1×10^{18} /cm^2 .

At present we are working towards the development of high voltage devices in SiC capable of withstanding voltages up to 2KV.

4H SiC Lateral RESURF Devices

Pronita Mehrotra, B. Jayant Baliga
Power Semiconductor Research Center
North Carolina State University
Raleigh, NC 27606

Introduction

SiC, due to its high bandgap, is an attractive material for devices used in high voltage, high temperature and high frequency applications. This work deals with development of SiC based lateral high voltage devices suitable for integration with CMOS circuits. The devices use the RESURF (REduced SURface Field) phenomena to improve the breakdown voltage by eliminating surface breakdown. Extensive work has been done in RESURF devices in Si [1-2], but it is still to be applied to devices in SiC. The goal of this report is to show simulation results for RESURF devices (diodes and MOSFETs) in 4H-SiC. Single zone diodes were extensively studied in a previous report [3]. This report will discuss simulations of double zone diodes and both single zone and double zone MOSFETs.

Double Zone RESURF diode

Fig.1 shows the cross-section of a lateral double zone RESURF diode. The basic structure consists of two p-n junctions: a vertical P^+N_{res1} junction and a horizontal P^-N_{res2} junction. The RESURF layer is split into two zones such that the dose in the second zone is three times the dose in the first zone. The advantage of splitting the RESURF zone into two sections is that the electric field profile becomes more uniform in the RESURF layer. This can be seen from Fig.2 which compares the electric fields inside the RESURF layer for a single zone and a double zone diode. For the single zone case, the electric field is high at the cathode and anode ends and dips considerably in the middle. With the introduction of the second zone, the electric field picks up again in the middle and the electric field is now more uniform. A more uniform electric field should result in the device supporting higher voltages. This phenomena has been reported earlier for Si devices [4].
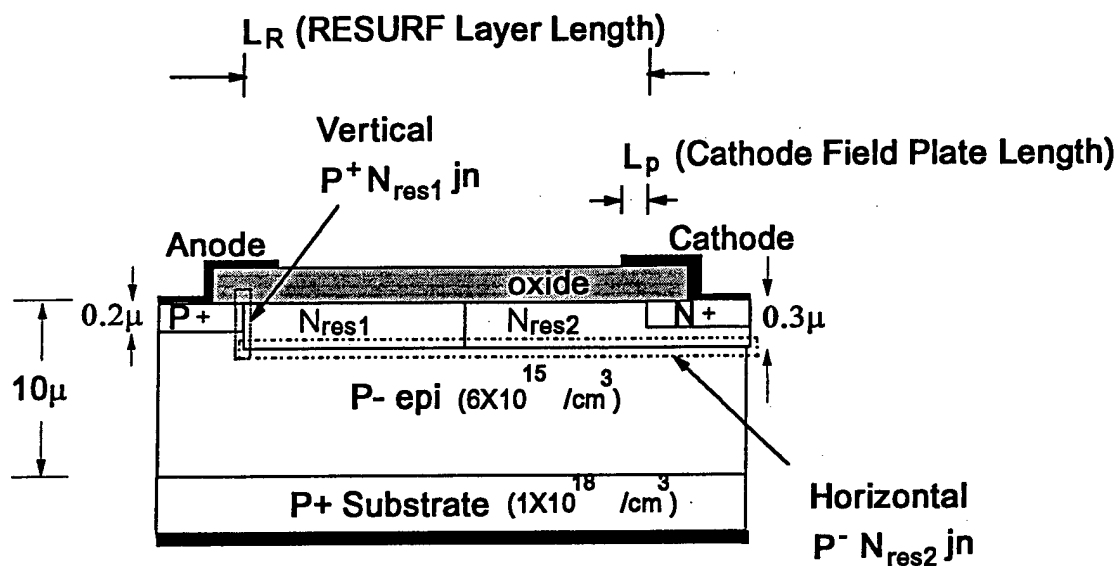
Fig 1 Cross-section of a double zone lateral SiC RESURF diode
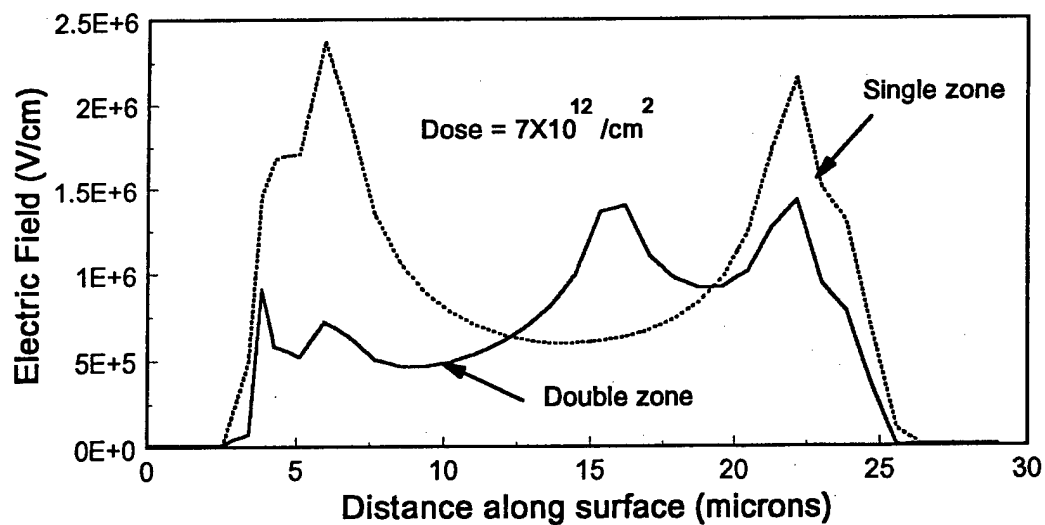

Fig 2 Electric Field at surface of a double zone RESURF diode

Our simulations for 4H SiC showed that not for all doses is the breakdown voltage improved for a double zone device. Fig. 3 shows the breakdown voltage vs. dose for the double zone case as compared to the single zone case. For low doses (<5e12 /cm^2), there is a marginal improvement in the breakdown voltage for the double zone case. For the dose range of 5e12-2.2e13 /cm^2, the breakdown voltage of the double zone diode is actually less than the single zone case. The reason why this happens is that the doping in the second zone becomes quite high and this half of the RESURF layer doesn't fully deplete. The effective RESURF length is therefore reduced, and hence, the voltage that can be supported in this region is reduced. At very high doses (> 2.2e13 /cm^2), the breakdown voltage improves by as much as 700V (at a dose of 3e13 /cm^2) . This is again because of a similar reason. For the single zone case, the doping is high and the depletion region doesn't even reach half the RESURF length. For the double zone case, since the doping in the first half is less than the doping of the single zone diode (to get the same average doping), the first half of the RESURF layer depletes fully and hence the effective RESURF length for the double zone case is now higher than the single zone case.
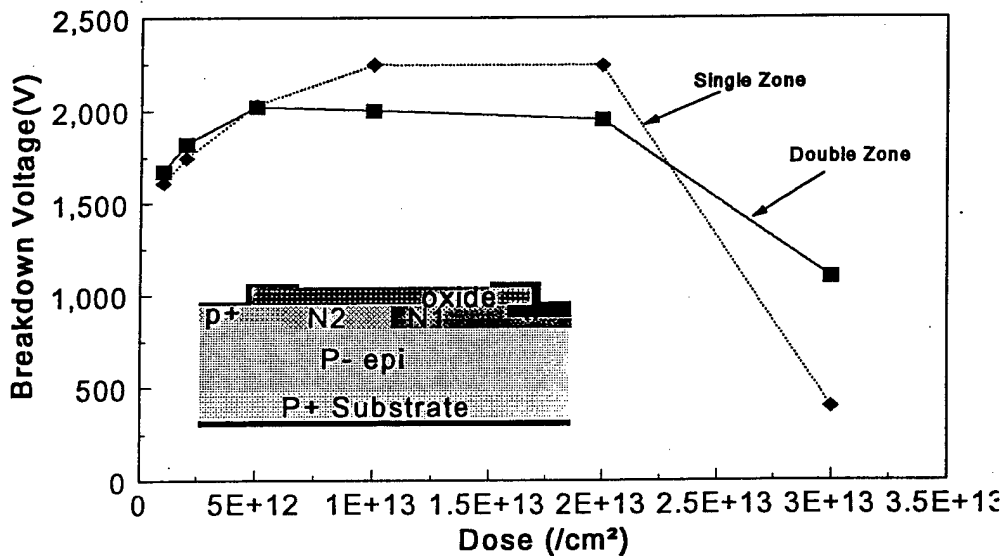

Fig 3 Breakdown Voltage of a double zone RESURF diode

4

Single Zone Accumulation Type RESURF MOSFET

Fig. 4 shows the device cross-section of the single zone Accumulation type RESURF MOSFET with a buried p+ region.
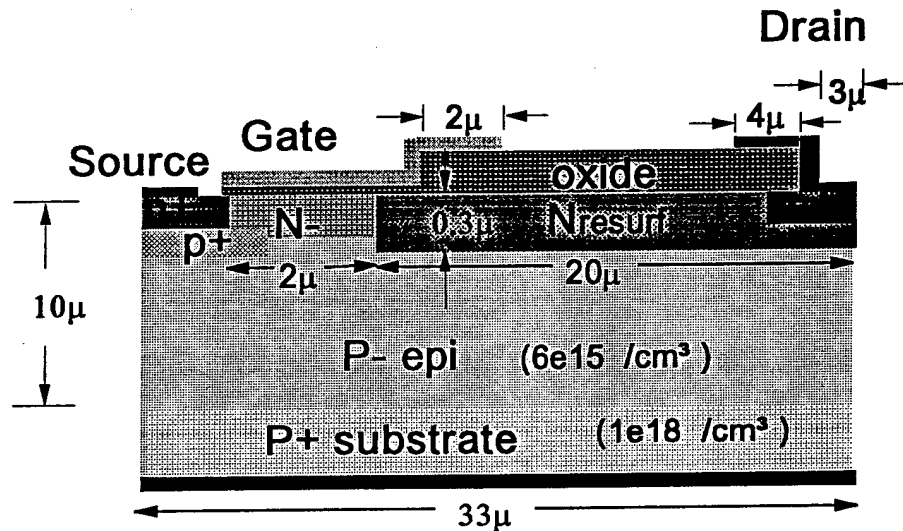

Fig 4 Cross-section of a single zone lateral SiC RESURF MOSFET with buried p+ region

Simulations were run for this device and RESURF behavior similar to that of the diode was observed. The device breaks down at low voltages for very high and very low RESURF doses and the breakdown voltage is quite high for optimum doses. In this case, we obtained high voltages (1700V-2000V) for a dose range of 2e12 - 1e13 /cm^2. The variation of breakdown voltage with dose is shown in Fig. 5. The MOSFET deviates in its behavior from the diode in that it has a low breakdown voltage (620V) at a dose of 2e13 /cm^2, as opposed to the diode which showed a high breakdown voltage up to 2e13/cm^2. Fig. 6a and 6b show the electric field profile in the RESURF region for a MOSFET and diode respectively, at a bias of 620V and a RESURF dose of 2e13 /cm^2. The peak electric field at the gate end in the MOSFET is higher than the peak electric field in the diode. This could be the reason that the MOSFET breaksdown even before the RESURF layer can get fully depleted.
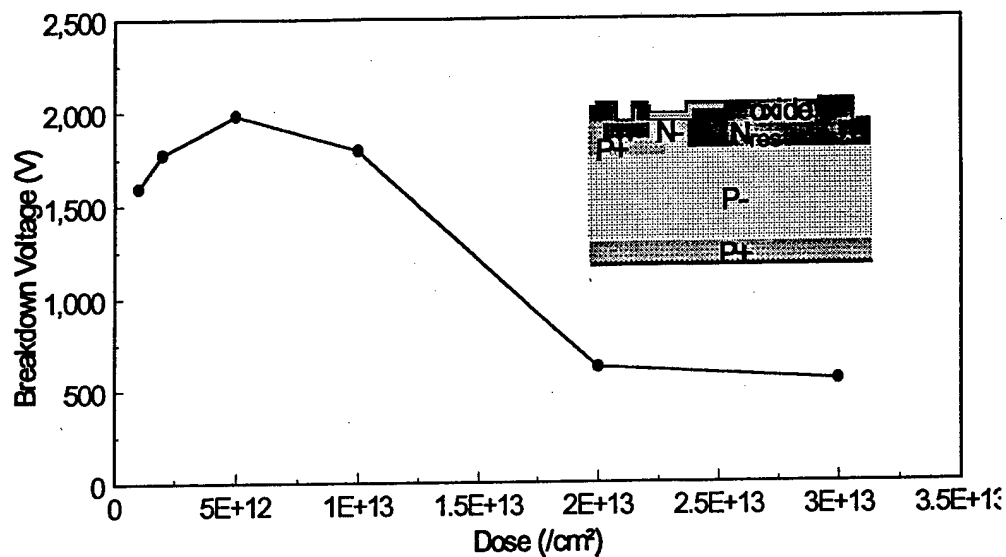
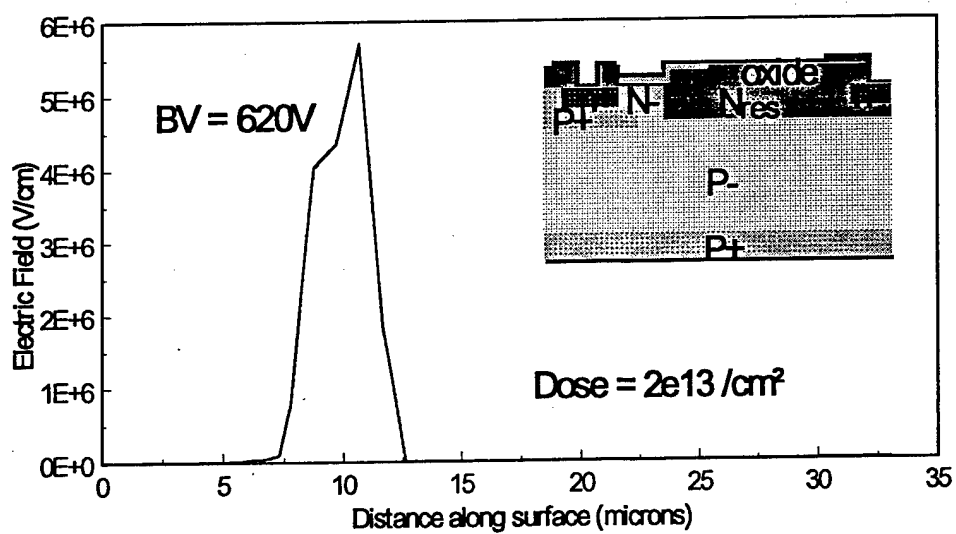*Fig 5 Optimization of RESURF dose for single zone accumulation type MOSFET*

Fig 6a Electric Field along surface for a single zone accumulation type MOSFET
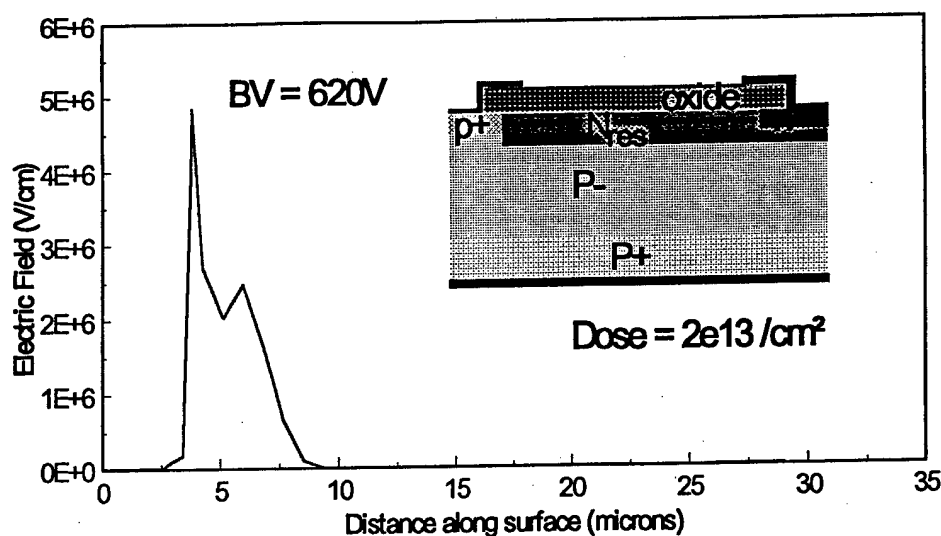
6

Fig 6b Electric Field along surface for a single zone diode

The specific on-resistance of the MOSFET also varies with the dose in the RESURF layer. For very low doses, the resistance of the RESURF layer becomes quite high and is the dominant component of the total specific on-resistance. For higher and higher doses, the total resistance falls and asymptotically starts approaching the channel resistance. The channel resistance component has been computed to be 7.6 mΩ-cm^2. Fig. 7 shows the change of total specific on-resistance with change in RESURF dose.
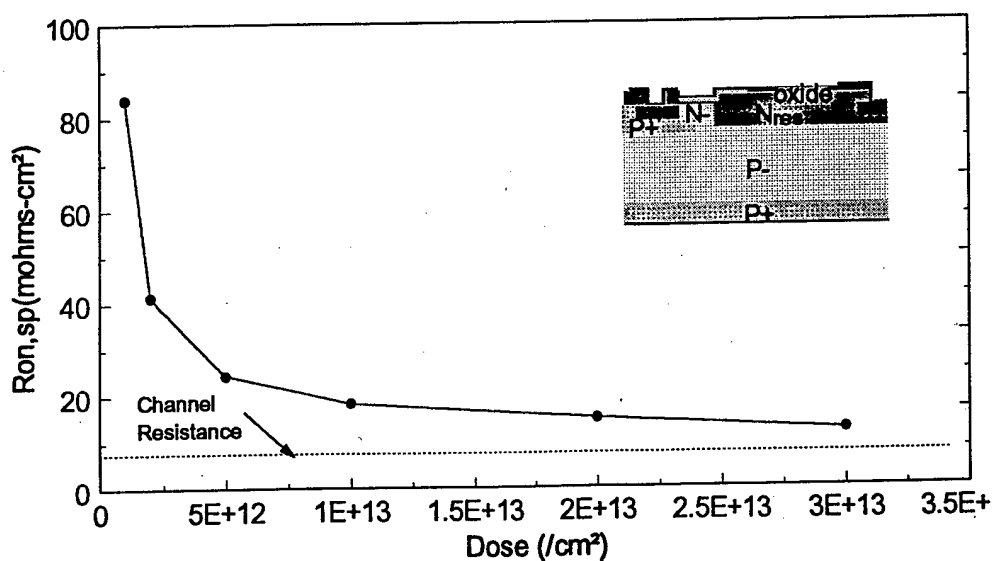

Fig 7 Specific on-resistance components for single zone accumulation type MOSFET

Fig. 8 shows the breakdown voltage vs. specific on-resistance for the single zone MOSFET. From the figure, it can be seen that for a breakdown voltage of 2000V, the specific on-resistance is 25 mΩ-cm^2. The specific on-resistance for a Si device for the same breakdown voltage is 400 mΩ-cm^2[5]. This gives an improvement of 16X for a SiC based device as opposed to a device made in Si. Care should be taken while designing the device to ensure that the device lies on the right half of the 25 mΩ-cm^2 point in Fig. 7 which would make the operation more stable. In the region left of this point, small process variations might make the device exhibit very low breakdown voltages.
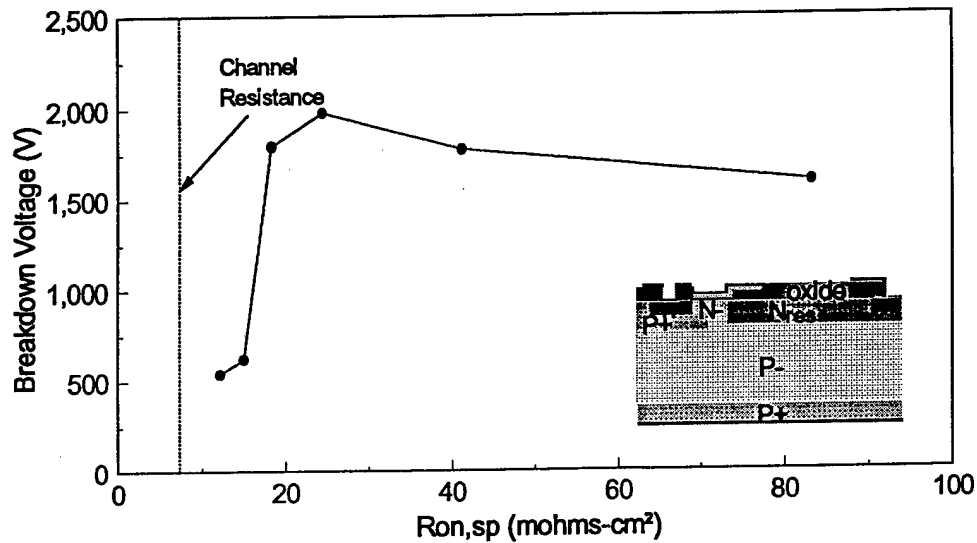

Fig 8 Optimization of RESURF dose for single zone accumulation type MOSFET

Simulations were then performed for a double zone accumulation type RESURF MOSFET. The double zone device showed improved breakdown voltage at a dose of 2e13 /cm^2. This is because, the lighter doped first half of the RESURF layer gets depleted faster and eliminates excessive field crowding at the gate end which resulted in premature breakdown in the single zone case. Fig. 9 shows the change in breakdown voltage with changing dose for the double zone MOSFET case and compares it with the single zone behavior.
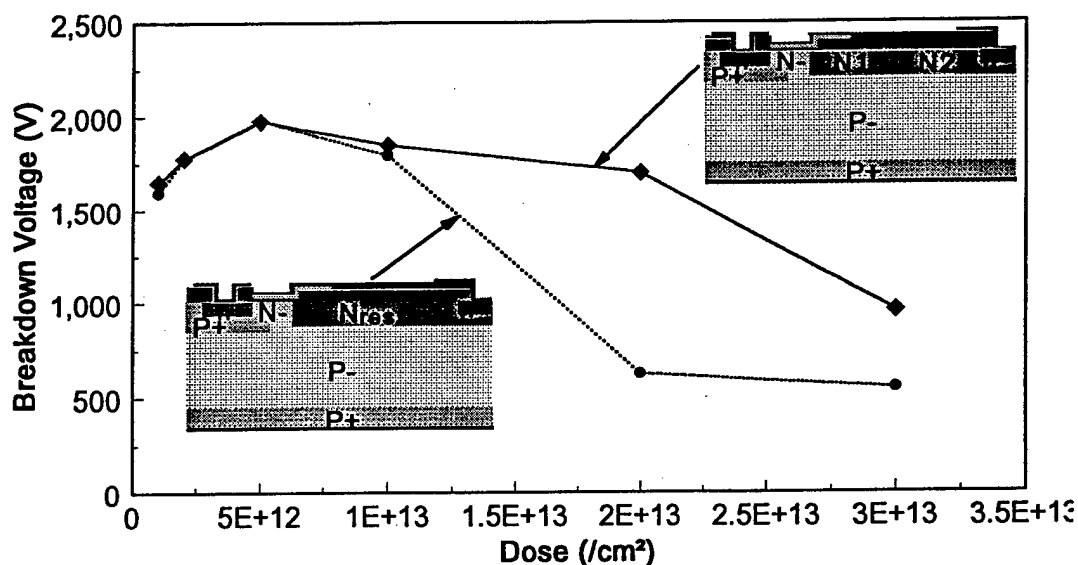
Fig 9 Optimization of RESURF dose for double zone accumulation type MOSFET

The specific on-resistance components of the double zone MOSFET is shown in Fig. 10. For low doses, the specific on resistance is higher for the double zone device as compared to the single zone device due to the splitting of the RESURF layer in to two zones. At higher doses, both the single zone and the double zone devices start approaching the channel resistance value.
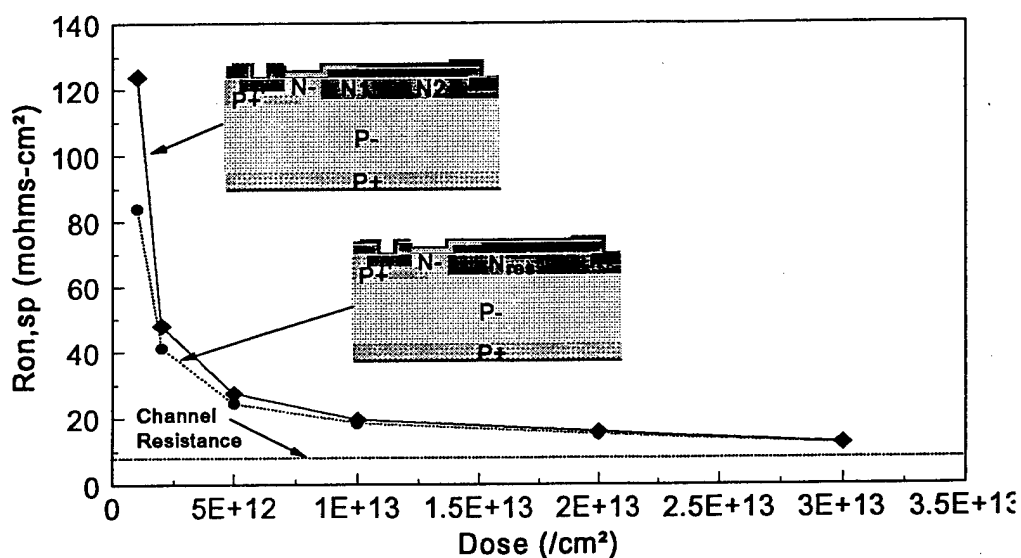

Fig 10 Specific on-resistance components for double zone accumulation type MOSFET

The breakdown voltage plotted against total specific on-resistance is shown in Fig. 11. From the figure, it can be seen that for a 2000V device, it is better to go for single zone devices as they offer a lower specific on-resistance. However, the curve to the left of the 2000V point falls less sharply for

the double zone device as compared to the single zone device, which suggests that it would be safer to make double zone devices as opposed to single zone devices.
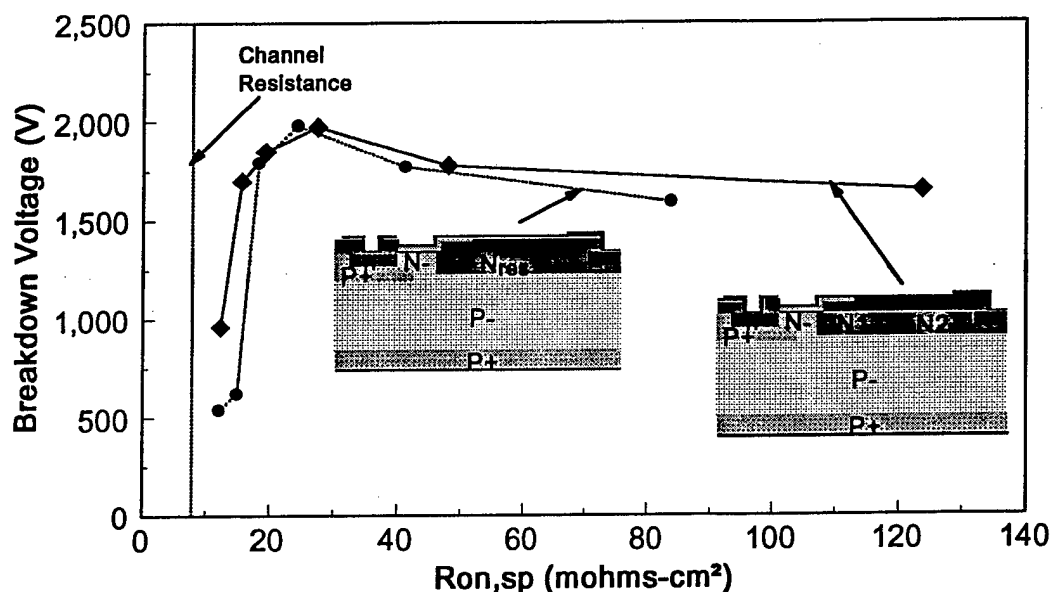

Fig 11 Optimization of RESURF dose for double zone accumulation type MOSFET

Simulations using Nitride

The main concern in fabricating RESURF devices in SiC is that the field in the oxide can become quite high and lead to oxide rupture. This problem has already been discussed in the previous report [3]. One of the approaches suggested to avoid this problem is to use a different dielectric like nitride which has a higher dielectric constant compared to oxide. We therefore, repeated simulations using nitride as the dielectric and these results are discussed next.

For the single zone RESURF MOSFET, simulations using nitride as the dielectric showed similar RESURF behavior. The absolute breakdown voltage for nitride was lower than for oxide. This can be seen from Fig.12 which shows the breakdown voltage plotted against the RESURF dose.
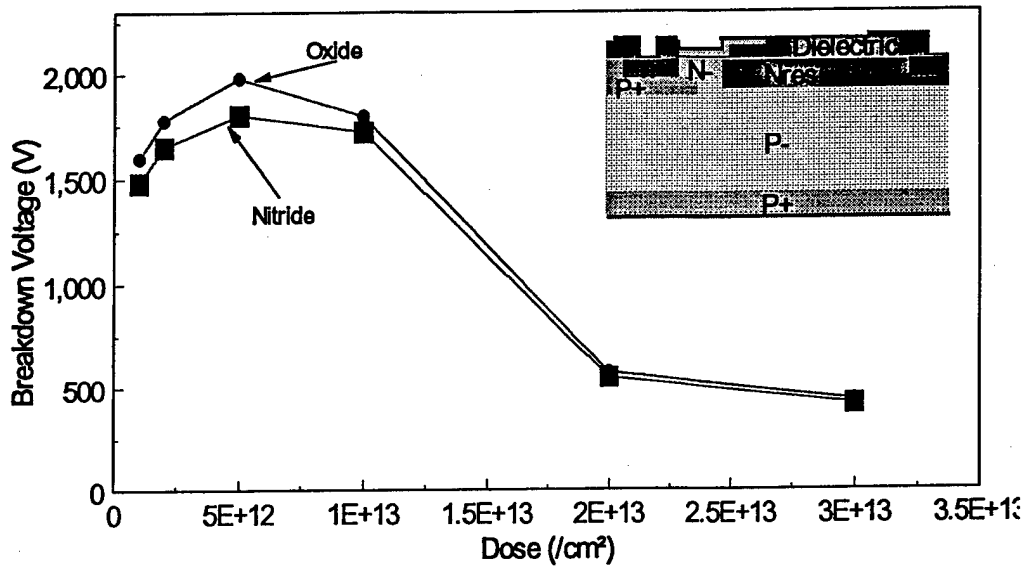
Fig 12 Optimization of RESURF dose for single zone MOSFET using nitride

The specific on-resistance for the two devices is shown in Fig.13. The specific on-resistance of the nitride case is lower than that of oxide. The channel resistance is given by

$$R_{ch} = \frac{L_{ch} \ t_d}{Z \ \mu_a \ \varepsilon_d (V_G - V_t)}$$

The dielectric constant, ε_d, for nitride is 7.5 whereas it is 3.85 for oxide. This accounts for the specific on-resistance being less for the nitride case. This effect if prominent only at high doses, when the channel resistance component becomes the dominant factor in the total on-resistance.
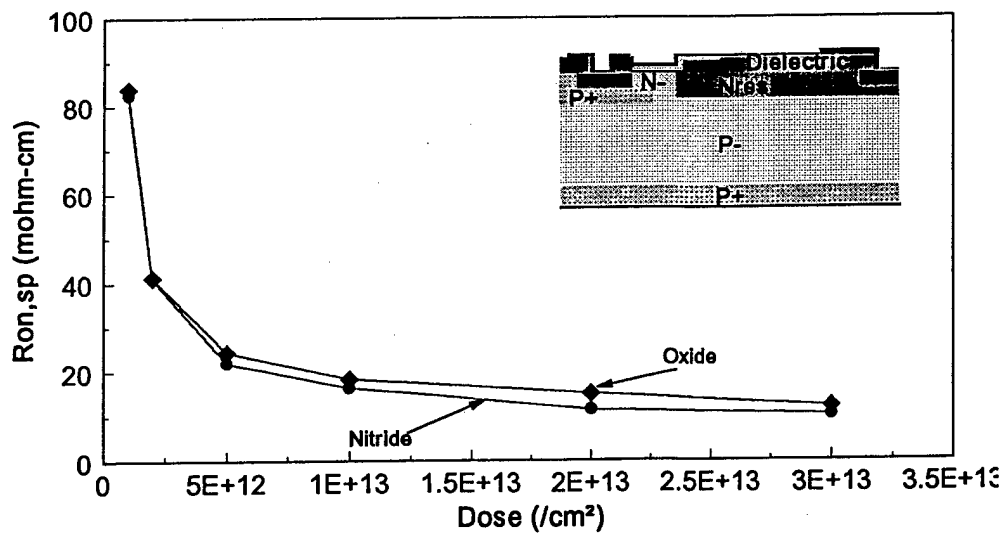

Fig 13 Specific on-resistance for single zone MOSFET using nitride

11

Finally, the breakdown voltage vs. specific on-resistance for the nitride case is plotted in Fig.14. The curves are similar in behavior and differ in the ways already pointed out. The nitride gives better on-resistance at high doses as compared to the oxide but maximum breakdown voltage obtained for the nitride was less than that of oxide. Devices fabricated in nitride should be more reliable because the peak electric field in nitride is less than that in oxide.
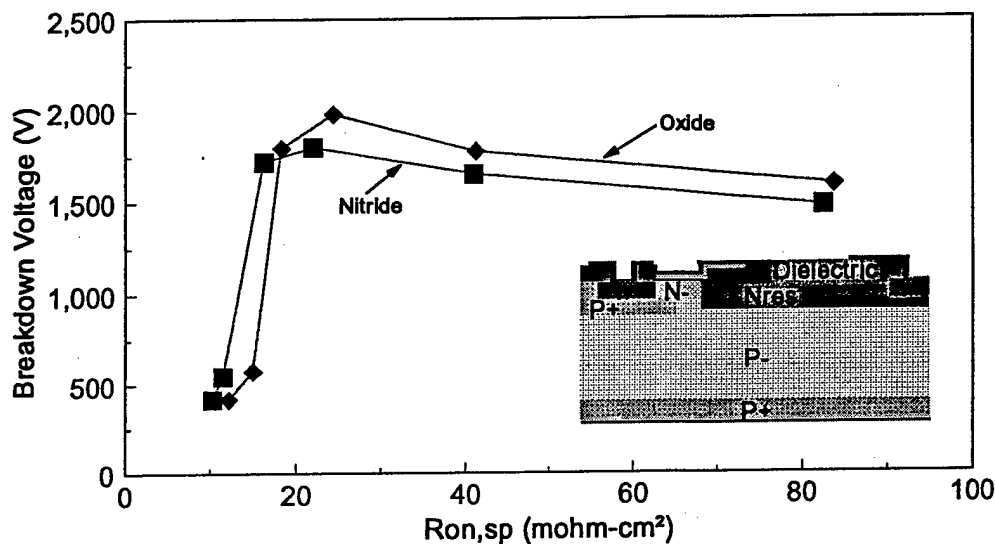

Fig 14 Optimization of RESURF dose for single zone MOSFET using nitride

Conclusions

Extensive numerical simulations were performed to study the behavior of RESURF devices (single and double zone diodes and MOSFETs) with both oxide and nitride. Oxide was found to be unacceptable as the field dielectric as the electric field in the oxide can become high enough to cause oxide rupture. Nitride is a better alternative as the field in the dielectric is lower due to its higher dielectric constant. For the diodes, double zone diode doesn't improve the breakdown voltage as compared to the single zone diodes in the range of interest. For MOSFETs, the breakdown voltage for the double zone case is improved considerably at high doses (up to 2e13 /cm^2) giving a very good range (5e12-2e13 /cm^2) where high breakdown voltages can be improved. However, a significant improvement in the performance is not obtained as this is offset by an increase in resistance. Devices with nitride as the dielectric exhibit behavior similar to devices with oxide. The key differences are that the maximum breakdown voltages obtained for nitride devices are lower than oxide devices. However, the on-resistance of the nitride devices are better than oxide devices at high doses.

References:
1) S. Merchant et al, *Proc. 3rd Int. Symp. On Power Semiconductor Devices and ICs (ISPSD)*, pp 31 (1991)
2) J.A. Appels and H.M.J. Vaes, *IEDM Tech. Digest*, pp 238 (1979)
3) Pronita Mehrotra and B.J. Baliga, *Tech. Report, PSRC Document:TR ,* (1998)
4) R. Sunkavalli et al, *Tech. Report, PSRC Document:TR-96-016*, (1996)
5) Amato and Rumennik, *IEDM Tech. Digest*, pp 736 (1985)

4H SiC Lateral RESURF Devices:

III. Device Design and Fabrication

A. Process Design:
To enable development of a silicon carbide technology similar to that now used to make silicon power ICs, we are working towards creating a planar technology for SiC using ion implantation to form all the regions in device structures. The process that we have defined in this project using SUPREM simulations allows the fabrication of lateral high voltage diodes and MOSFETs using process steps similar to those used today for manufacturing silicon devices. The only exception is the need to anneal the ion implants at much higher temperatures (near 1650^0C). This process flow contains 75 major steps.

B. Mask Design
A mask set has been designed for the fabrication of a variety of devices based upon the above process flow. The designs include high voltage RESURF (reduced surface electric field) diodes and high voltage RESURF MOSFETs with different drift region lengths. Two types of novel accumulation channel MOSFET designs have been included together with the conventional inversion channel MOSFETs. This will enable fabrication of devices with voltage ratings ranging from 200 to 2000 volts. In addition, we hve designed CMOS devices to examine the campatibility for integration of logic circuits with the power devices.

C. Wafer Procurement
The fabrication of the RESURF devices will be done by ion implantation of N-type dopants into a P-type substrate to create the drift region. This method allows precise control of the charge in the drift region via the ion implant dose, while giving the flexibility to vary the dose from wafer to wafer to study its impact on the RSURF phenomenon. For this purpose, the starting material was chosen to be 10 micron thick p-type epitaxial layers with doping concentration of 1×10^{16} cm^{-3} grown on P+ 4H-SiC wafers. These wafers were ordered from CREE Research Inc. in time to begin device fabrication as soon as the mask and process designs were completed.

D. Device Fabrication
The fabrication of the RESURF devices has been started. Four wafers were included in this run to enable varying the RESURF dose in the range of 1×10^{12} cm^{-2} to 4×10^{13} cm^{-2} At this time, we have completed up to process step 15 out of the 75 total process steps. This includes the first deep Boron implant to create the buried P+ layer for the accumulation channel devices.

14